

FIG. 3

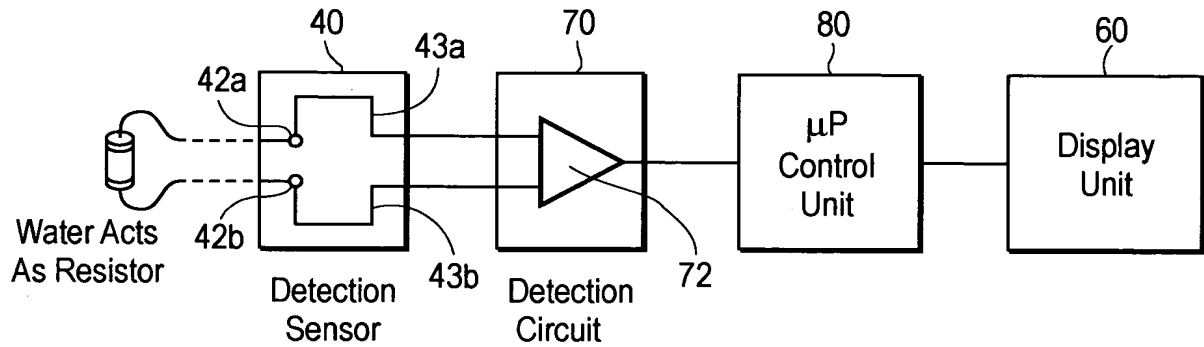


FIG. 4A

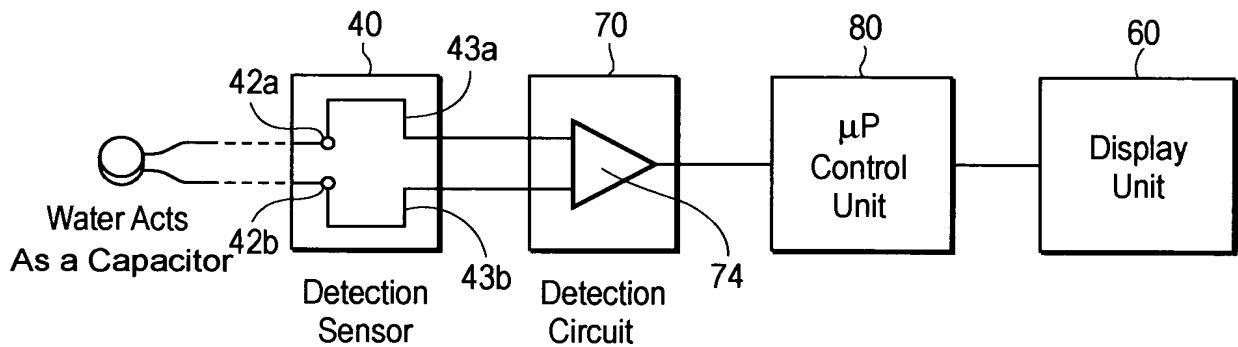


FIG. 4B

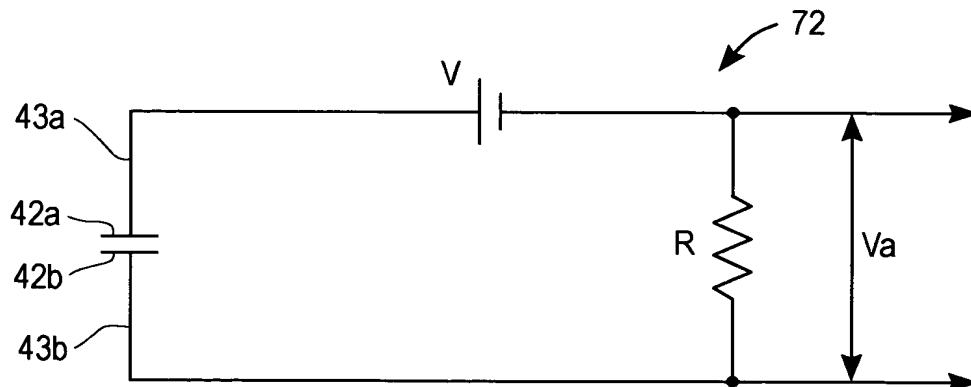
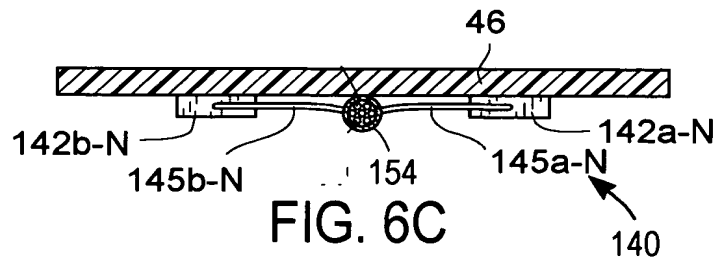
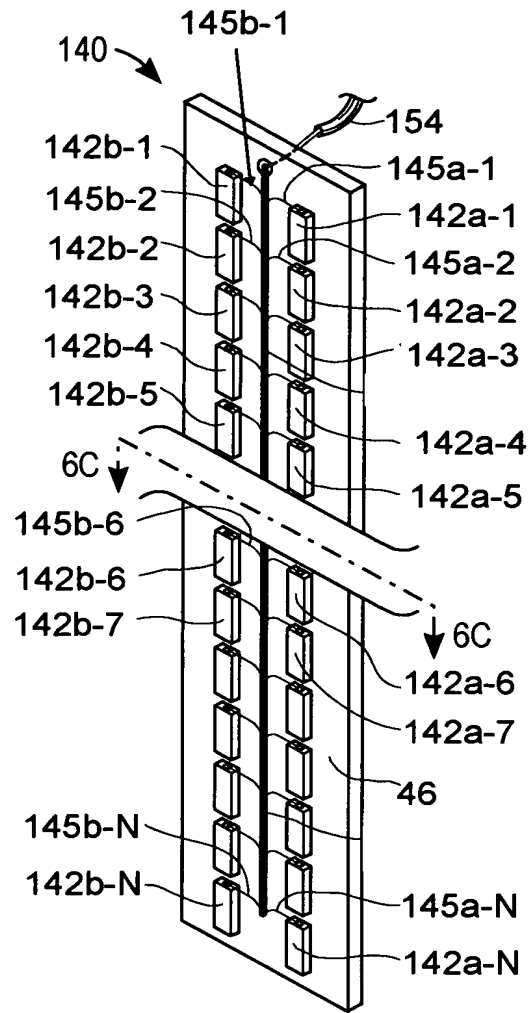
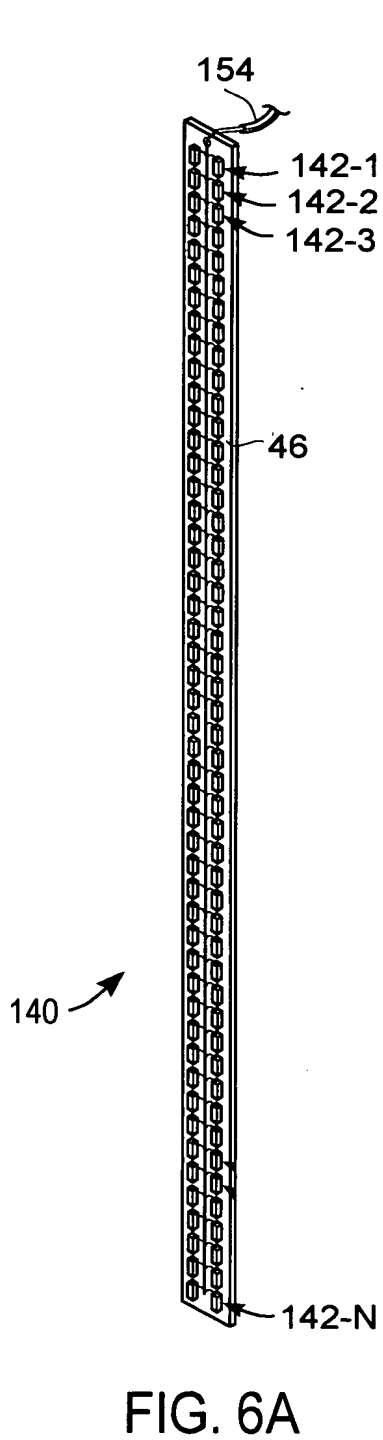


FIG. 5



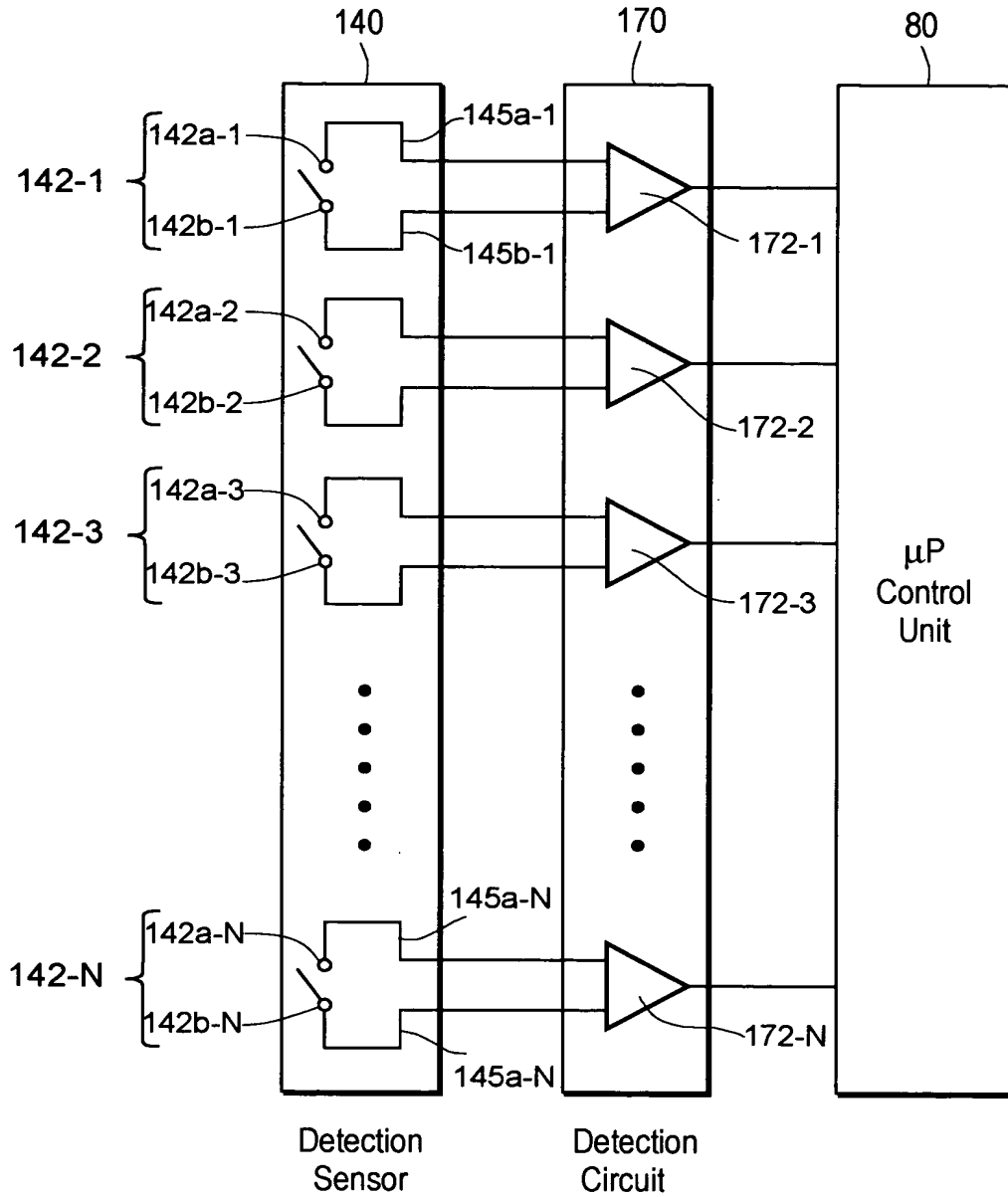


FIG. 7

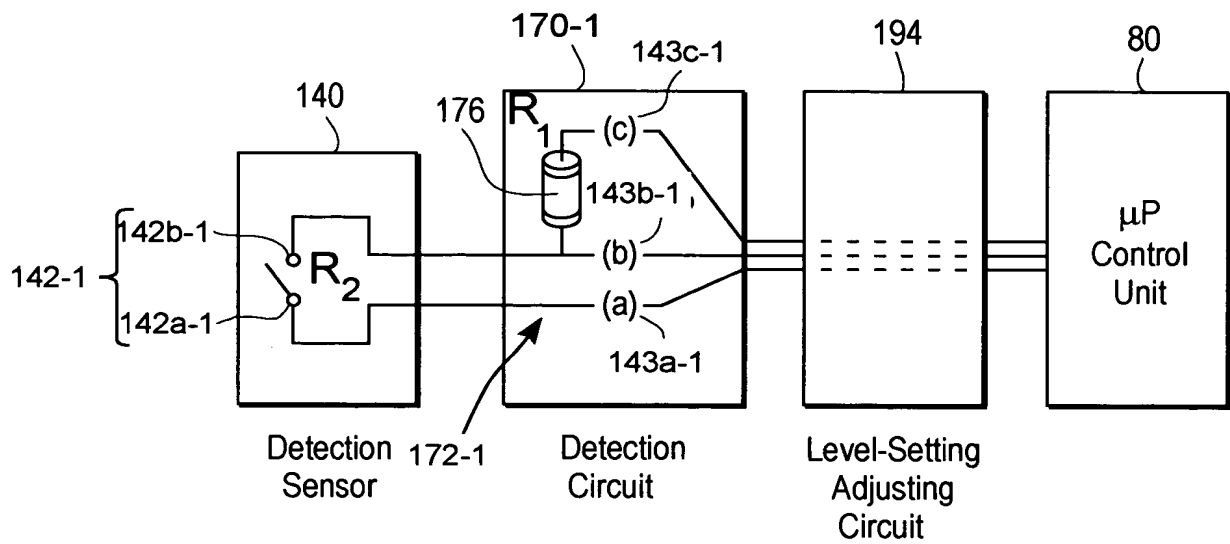


FIG. 8

		144	180	144a	144b	144c
Time	Water Level	Switch	Microprocessor	(a)	(b)	(c)
t0	Low	Open	Off	0	1	1
•						
t1	Low	Open	Off	0	1	1
•						
t2	High	Closed	On	0	0	1
t3	High	Closed	On	1	0	0
t4	High	Closed	Off	1	1	0
•						
t5	Low	Open	On	1	0	0
t6	Low	Open	On	0	0	1
t7	Low	Open	Off	0	1	1
•						
t8	High	Closed	On	0	0	1
t9	High	Closed	On	1	0	0
t10	High	Closed	Off	1	1	0
•						

FIG. 9



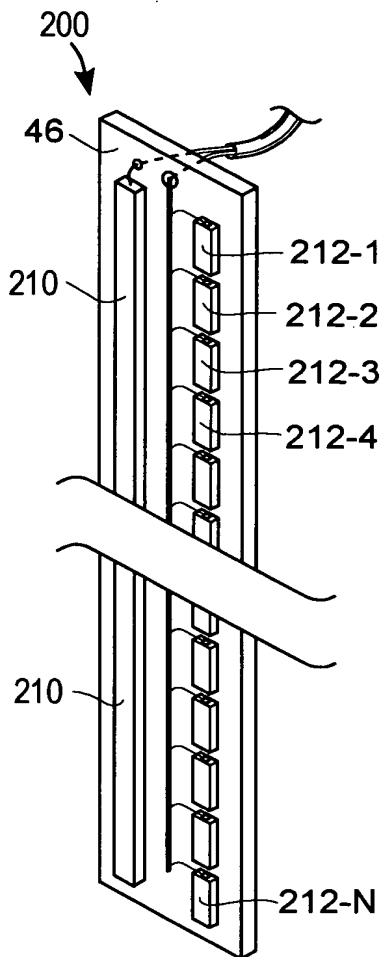


FIG. 10

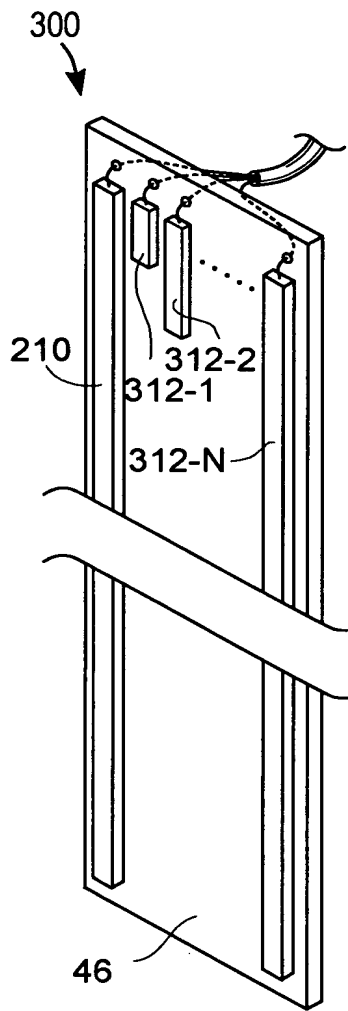


FIG. 11

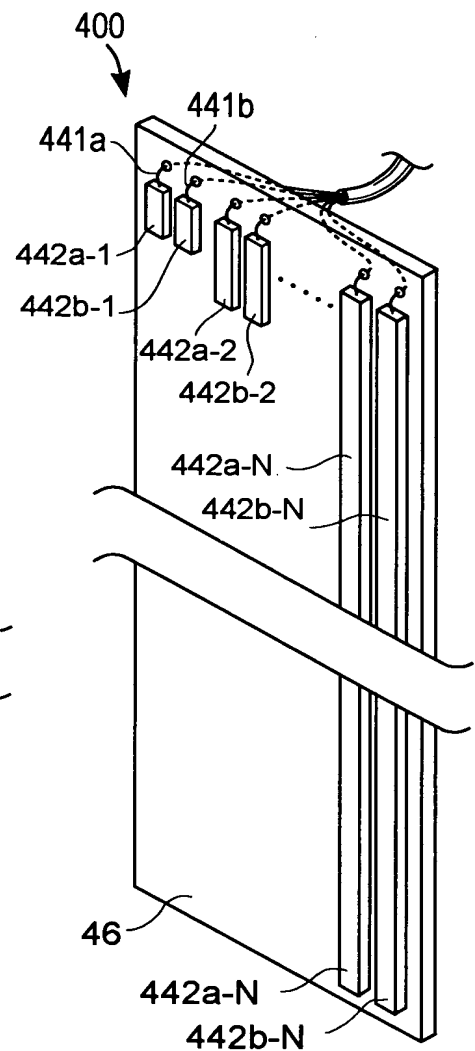


FIG. 12

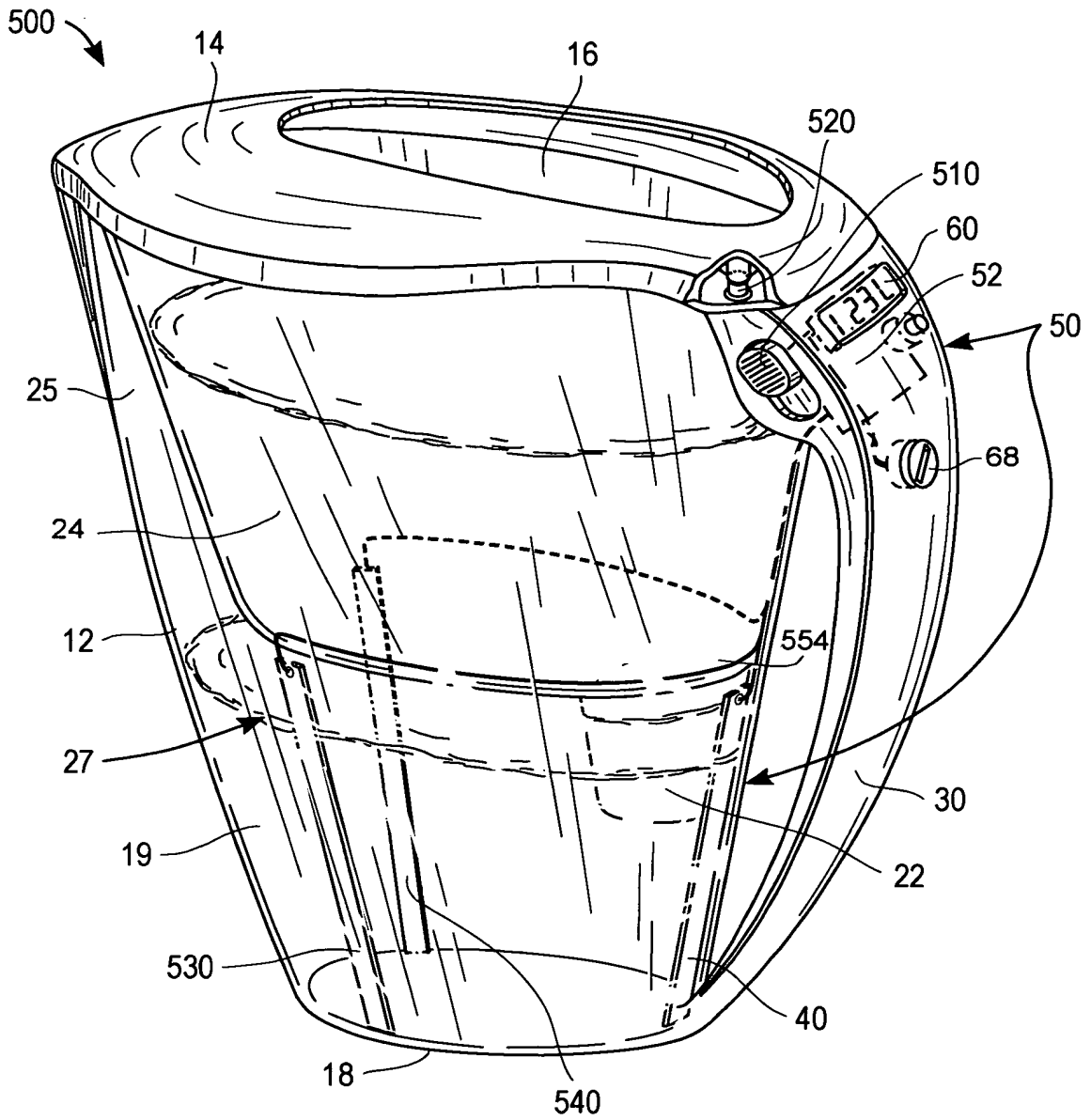


FIG. 13

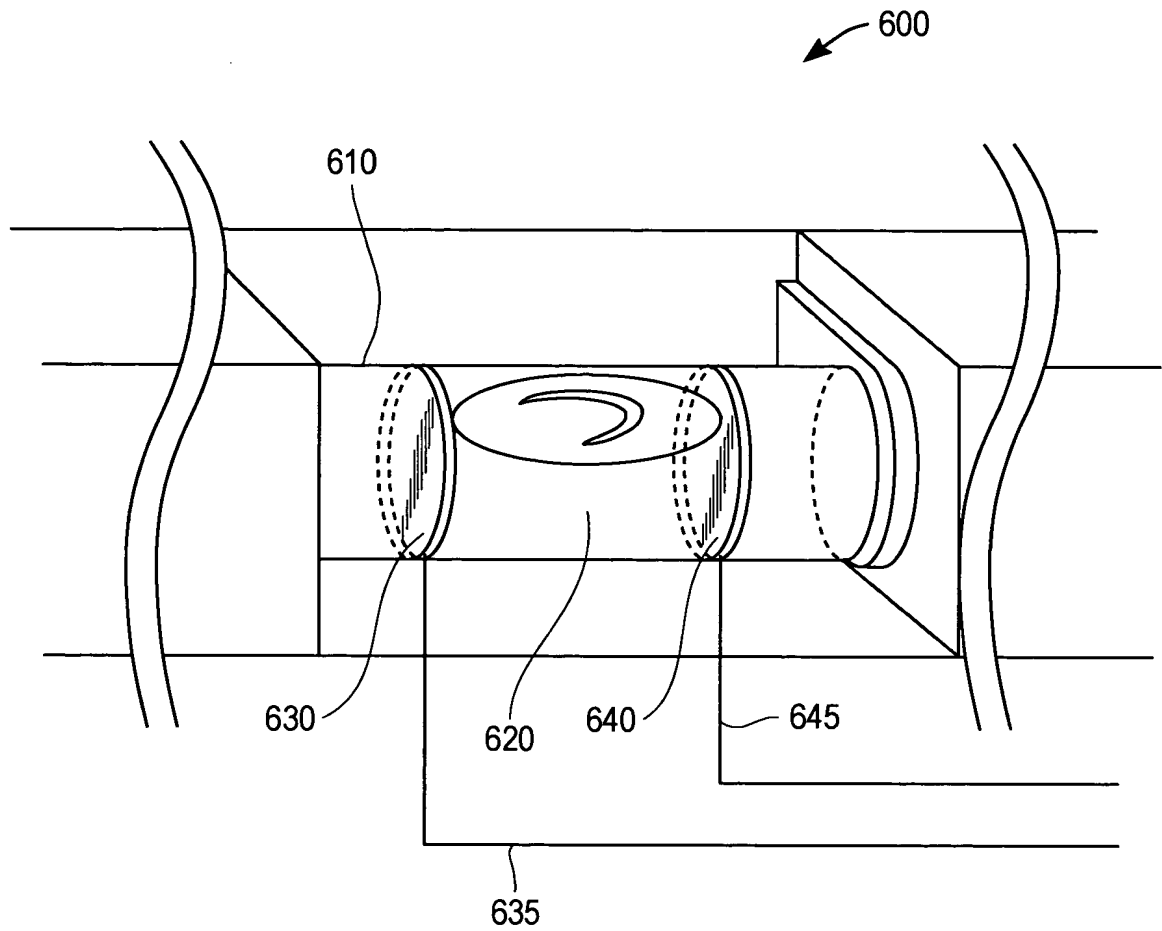


FIG. 14